

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION**

ACQIS LLC,	§	
Plaintiff,	§	
	§	
	§	
vs.	§	
	§	
ASUSTEK COMPUTER, Inc.,	§	Civil Action No.: 6:20-cv-965-ADA
Defendant,	§	
	§	
INVENTEC CORPORATION,	§	Civil Action No.: 6:20-cv-966-ADA
Defendant,	§	
	§	
LENOVO GROUP LTD. et al,	§	Civil Action No.: 6:20-cv-967-ADA
Defendants,	§	
	§	
MITAC COMPUTING TECHNOLOGY	§	Civil Action No.: 6:20-cv-962-ADA
CORPORATION,	§	
Defendant,	§	
	§	
WIWYNN CORPORATION,	§	
Defendant.	§	Civil Action No.: 6:20-cv-968-ADA
	§	

DEFENDANTS' OPENING CLAIM CONSTRUCTION BRIEF

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I. INTRODUCTION

In these consolidated cases—ACQIS’s latest campaign to assert a large group of closely related patents reciting different permutations of the same claim terms—ACQIS attempts to re-litigate issues already resolved in other district courts and that are now before the Federal Circuit. For the reasons set forth in Defendants’ Motion to Stay (Dkt. No. 71 (No. 6:20-cv-00967)), these consolidated cases should be stayed pending the forthcoming decisions of the Federal Circuit in *ACQIS LLC v. EMC Corp.*, No. 21-1772 (Fed. Cir. Mar. 24, 2021) and the Eastern District of Texas in *ACQIS LLC v. Samsung Elecs. Co., Ltd., et al.*, No. 2:20-cv-00295 (E.D. Tex. Sept. 3, 2020). Those decisions will address nearly all the same claim terms proposed for construction here, and most importantly, the “Peripheral Component Interconnect (PCI) bus transaction” term recited in 95 of the 129 asserted claims.

In seeking out yet another forum to construe the exact same claim terms, ACQIS attempts to backtrack from positions it has taken in prior district court proceedings, and before the Patent Office, which are now part of the intrinsic record. *Aylus Networks, Inc. v. Apple Inc.*, 856 F.3d 1353, 1361 (Fed. Cir. 2017). ACQIS’s goal in revisiting the prior constructions is transparent—to discard clear limitations of the alleged invention to maintain its infringement read, despite having relied on those same limitations to distinguish the prior art.

If these cases are not stayed, this Court should adopt the Defendants’ proposed claim constructions, which are consistent with the well-reasoned opinions of other district courts addressing the same patents or related patents. In short, Defendants’ constructions properly reflect the entirety of the intrinsic record—that is, ACQIS’s repeated admissions before the Patent Office, as well as the plain language of the claims and the disclosures of the patent specifications.

II. BACKGROUND

ACQIS currently asserts 15 patents¹ and 129 claims against the 11 consolidated Defendants. *See e.g.*, Dkt. 1, Nos. 6:20-cv-00962, 65-68; Ex. 1 (Asserted Patents and Asserted Claims). The patents fall broadly into two related families (the Non-Reissue Asserted Patents and Reissue Asserted Patents) which share common parent applications filed by the same inventor, rely on the same subject matter purportedly incorporated by reference from the same unrelated applications, and describe virtually identical subject matter. *See* Ex. 2 (Family Tree of Asserted Patents). The large number of patents is the result of ACQIS's decades-long practice of filing extensive continuation applications in order to capture later technological advancements.

The ACQIS patents describe a “modular” computer system that combines well-known technology, namely, a “**computer module**” that houses a CPU and memory, and inserts into a “**console**” that connects peripheral devices (*e.g.*, monitor, keyboard, mouse, modem, etc.) to form a fully functional computer.

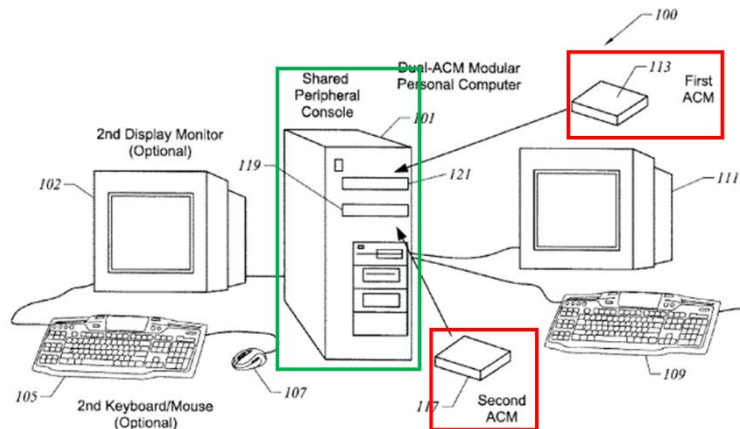


FIGURE 1

E.g., '873 patent at 9:41–10:18; Fig. 1

(shown); '739 patent at 7:64–8:24; Fig. 1. ACQIS's alleged invention was an improvement to the way existing computer modules and peripheral consoles communicated with each other, and in

¹ The asserted patents are U.S. Patent Nos. 7,676,624 (the “624 patent”), 8,041,873 (the “’873 patent”), 8,626,977 (the “977 patent”), 8,977,797 (the “797 patent”), 8,756,359 (the “359 patent”), 9,529,768 (the “768 patent”), 9,703,750 (the “750 patent”), and 9,529,769 (the “769 patent”) (collectively, the “Non-Reissue Asserted Patents”); and U.S. Patent Nos. RE43,602 (the “602 patent”), RE44,468 (the “468 patent”), RE44,739 (the “739 patent”), RE46,947 (the “947 patent”), RE44,654 (the “654 patent”), RE45,140 (the “140 patent”) (collectively, the “Reissue Asserted Patents”).

particular, communication via a well-known industry standard interface called the “Peripheral Component Interconnect (“PCI”) bus.” The “computer module” provides portability, having an enclosure and console connectors that allow a user to easily insert and remove it from the “console.” The requirements for PCI bus-type communications are defined in the PCI Local Bus Specification, which is referenced in every patent as admitted prior art. *E.g.*, ’873 patent at 3:14; ’739 patent at 3:26.

As the patents explain, the PCI Local Bus Specification requires communication via “parallel” signal lines:

[A]s a result of operating by PCI protocols, the prior art interface includes a very large number of signal channels with a corresponding *large number of conductive lines (and a similarly large number of pins in the connectors of the interface)* that are commensurate in number with the number of signal lines in the PCI buses which it interfaces.

E.g., ’873 patent at 3:48–54.² The patents describe “parallel” communication as disadvantageous because “it costs more,” “is bulkier and more cumbersome to handle,” and makes less viable “using differential voltage signals,” which “is more cable friendly, faster, consumes less power, and generates less noise.” *E.g.*, ’873 patent at 3:54–66. On the other hand, as ACQIS acknowledged in a related *Inter Partes Review* (“IPR”), “PCI had been widely adopted” and the industry “would not easily abandon it”; thus, ACQIS’s aim was to “develop[] a system to speed up PCI transactions that was completely compatible with existing peripheral devices.” Ex. 3 (*EMC Corp. v. ACQIS LLC*, IPR2014-01462, Paper 30 (“’873 IPR ACQIS Resp.”)), at 3. ACQIS explained: “*key to the invention was to serialize the otherwise parallel PCI bus transactions* to increase communication speeds.” *Id.*

² All emphases have been added unless otherwise noted.

In this regard, the patents describe a purportedly new interface for transmitting existing parallel PCI bus transactions in serial form. The patents explain: “ACM [attached computer module] 605 and the peripheral console 610 are interfaced through an exchange interface system (XIS) bus 615” which “includes power bus 616, video bus 617 and peripheral bus (XPBus) 618.” *E.g.*, ’873 patent, 15:1–5; Fig. 6. For transmission over ACQIS’s XPBus, the PCI bus transactions—including all PCI address, data and control signals—are encoded for conversion from parallel to serial form. *See, e.g.*, ’873 patent, 16:55–58 (“**Encoders . . . format the PCI address/data bits** to a form more suitable for parallel to serial conversion prior to transmittal on the XPBus.”); *see also id.* 17:23–28 (“Control encoder & merge data path unit 1025 **encodes PCI control signals . . . into control bits**, . . . then transmits the control bits on the data lines PD0 to PD3 and control line PCN of the XPBus.”).

Importantly, even with ACQIS’s serial interface (the XPBus), existing computer modules and peripheral consoles would continue to use the PCI Local Bus Specification internally. Ex. 3 (’873 IPR ACQIS Resp.), at 2–3, 8–10. That meant preserving the entirety of the PCI standard transaction “so that the serialized communications were compatible with existing peripheral devices.” *See id.* at 3, 10; *see also* Ex. 4 (*EMC Corp. v. ACQIS LLC*, IPR2014-01462, Paper 60 (“IPR Hr’g Tr.”)), at 31:18–32:4.

Accordingly, ACQIS’s purported invention (1) connects computer modules and peripheral consoles that implement PCI standard transactions; (2) converts parallel PCI standard transactions into serial form for transmission over a serial interface; and (3) preserves the PCI standard transaction for subsequent communications in the modules and consoles.³

³ To the extent that the patents address non-PCI bus transactions, *e.g.*, USB transactions, the specification refers to known serial communications for connecting peripheral devices. *E.g.*, ’873

III. ARGUMENT

A. The Case Dispositive “PCI” Claim Constructions of the EMC Litigation Are Fully Consistent with the Intrinsic Record and Should Be Adopted

In ACQIS’s litigation against EMC Corporation (“EMC” and the “EMC Litigation”), two District Court judges correctly construed the term “PCI bus transaction” as a transaction that operates “in accordance with the industry standard PCI Local Bus Specification.” ACQIS asks this Court to depart from the *EMC* constructions—by disregarding fundamental elements of a PCI standard transaction and ignoring the intrinsic record—in order to capture the Peripheral Component Interconnect *Express* (“PCIe”) Specification, which was released years after ACQIS’s purported invention and differs fundamentally from the claimed PCI Local Bus Specification.

In short, ACQIS requests that the Court modify the *EMC* constructions to overcome a non-infringement problem resulting from the allegedly infringing products’ compliance with the PCIe Specification. But that request is contrary to the canons of claim construction. *See Source Vagabond Sys. Ltd. v. Hydrapak, Inc.*, 753 F.3d 1291, 1299–1300 (Fed. Cir. 2014) (“[A]n ‘analysis’ that adds words to the claim language without support in the intrinsic evidence in order to support a claim of infringement does not follow standard canons of claim construction.”) (internal quotation marks and brackets omitted); *Iris Connex, LLC v. Acer Am. Corp.*, No. 2:15-cv-1909, 2016 WL 4596043, at *13 (E.D. Tex. Sept. 2, 2016) (rejecting proposed construction that was “directed at construing the claim so that it reads on the accused device”).

1. The EMC Court Correctly Construed the Disputed PCI Terms, Including by Adopting Constructions Agreed to by ACQIS

In 2013, ACQIS filed suit against EMC and several other defendants in the Eastern District of Texas. There, Judge Davis construed “Peripheral Component Interconnect (PCI) bus

patent, 11:37-42 (“The secondary ACM 219 accesses peripheral devices [through] the Ethernet connection . . . and can use other high-speed serial communication such as USB 2.0, and 1394.”)

transaction” as “information, in accordance with the PCI standard, for communication with an interconnected peripheral component.” *ACQIS LLC v. Alcatel-Lucent USA Inc., et al.*, No. 6:13-cv-638, 2015 WL 1737853, at *5 (E.D. Tex. Apr. 13, 2015) (“*EMC E.D. Tex. Markman*”). Judge Davis also made clear that “a PCI bus transaction must include *all* information required by the PCI standard,” not just the subset of information ACQIS proposed: the “digital command,” “address,” and “data information.” *Id.* at *5.

Judge Davis then transferred ACQIS’s case against EMC to the District of Massachusetts. *ACQIS LLC v. EMC Corp.*, 67 F. Supp. 3d 769, 774 (E.D. Tex. 2014). Following a stay pending *IPR*, Judge Burroughs further held claim construction proceedings in the District of Massachusetts. ACQIS proposed that “PCI bus transaction” be construed as “information, in accordance with the PCI Standard, for communicating with an interconnected peripheral component.” *ACQIS, LLC v. EMC Corp.*, No. 14-cv-13560, 2017 WL 6211051, at *3 (D. Mass. Dec. 8, 2017) (“*EMC D. Mass. Markman*”). Judge Burroughs adopted a modification of the construction *with ACQIS’s agreement*: “a transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component.” *Id.* at *3, 5. This construction of “PCI bus transaction” proved case dispositive.

EMC moved for summary judgment of non-infringement on the basis that EMC’s products did not operate in accordance with the industry standard PCI Local Bus Specification. *ACQIS, LLC v. EMC Corp.*, No. 14-cv-13560, 2021 WL 1088207, at *3-4 (D. Mass. Feb. 19, 2021) (“*EMC D. Mass. Summary Judgment*”). In particular, EMC argued that a transaction in accordance with the PCI Local Bus Specification, *i.e.*, a PCI standard transaction, requires not only (1) address, data and command information, as ACQIS contended, but also (2) address and data phases, as well as control and parity signals. *Id.* at *4. It was undisputed that the EMC products did not implement

PCI standard transactions. ACQIS—as it did before Judge Davis and as it does now—attempted to rewrite the requirements of the PCI Local Bus Specification by arguing that address and data phases, and control and parity signals are “outside the scope of the PCI bus transaction itself.” *Id.* Judge Burroughs dismissed ACQIS’s infringement arguments as “attempts to skirt the claim construction set forth by Judge Davis and this Court.” *Id.*

2. The Shared Ancestry and Common Claim Terms of the Asserted Patents Require Constructions Consistent with Those Entered in the EMC Litigation

Four of the fifteen patents asserted in these consolidated cases were also asserted against EMC.⁴ The remaining eleven asserted patents are closely related to the four asserted against EMC as they (1) belong to the same patent families, (2) have the same, sole inventor, (3) concern the same subject matter, (4) contain many near-identical claim limitations (as illustrated below), and (5) all purport to claim priority to a common application, U.S. Patent No. 6,718,415, or are reissues of U.S. Patent No. 6,643,777. *See* Ex. 2 (Family Tree of Asserted Patents).

Exemplary Claim Comparison Table	
Claim 60 of US 7,363,416 Asserted Against EMC	Claim 11 of US 7,676,624 Asserted Against Defendants
56. A computer system comprising: a console comprising an Ethernet hub controller, a first coupling site and a second coupling site, the console being an enclosure housing the Ethernet hub controller, the coupling sites, and a plurality of computer modules, each coupled to one of the coupling sites; each computer module comprising a processing unit, a main memory coupled to the processing unit, an interface controller coupled to a differential signal channel of two unidirectional serial bit	11. A computer system comprising: a console comprising a first coupling site and a second coupling site, each coupling site comprising a connector; the console being an enclosure housing each coupling site; a plurality of computer modules, each computer module coupled to one of the coupling sites through the connector, and comprising a processing unit, a main memory coupled to the processing unit, and an interface controller coupled to a differential signal channel comprises two

⁴ The overlapping patents are U.S. Patent Nos. 7,676,624; 8,041,873; RE42,984; and RE44,468.

streams which transmit data in opposite direction for communicating encoded serialized <u>Peripheral Component Interconnect (PCI) bus transaction</u> data to a connector, and an Ethernet controller coupled to the Ethernet hub controller for communication between the computer modules; wherein each of the computer modules operates fully independent of each other.	sets of unidirectional low voltage serial bit channels in opposite directions transmitting encoded <u>PCI bus transaction</u> data; wherein each of the computer modules operates fully independent of each other, and wherein the interface controller couples to the console through the differential signal channel for data communication, through the connector of the coupling site.
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“The same claim term in the same patent or related patents carries the same construed meaning.” *In Re Rambus Inc.*, 694 F.3d 42, 48 (Fed. Cir. 2012) (quoting *Omega Eng’g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1334 (Fed. Cir. 2003)); *see also SightSound Techs., LLC v. Apple Inc.*, 809 F.3d 1307, 1316 (Fed. Cir. 2015) (“Where multiple patents ‘derive from the same parent application and share many common terms, we must interpret the claims consistently across all asserted patents.’”) (citations omitted); *In re Katz Interactive Call Processing Pat. Litig.*, 639 F.3d 1303, 1325 (Fed. Cir. 2011) (“[W]e ordinarily interpret claims consistently across patents having the same specification.”); *Abtox, Inc. v. Exitron Corp.*, 131 F.3d 1009, 1010 (Fed. Cir. 1997) (“Although these claims have since issued in separate patents, it would be improper to construe this term differently in one patent than another, given their common ancestry.”). Accordingly, the *EMC* constructions—which are grounded in the intrinsic and extrinsic records, as confirmed by ACQIS’s own admissions—should apply to the asserted patents here because four patents are identical and the remaining patents claim priority to common applications, have substantially the same specifications, and share the disputed claim terms.

B. “PCI Bus Transaction” Terms

1. “Peripheral Component Interconnect (PCI) Bus Transaction” / “PCI Bus Transaction”⁵

Defendants’ Proposed Construction	ACQIS’s Proposed Constructions
“a transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component”	“information, including at least PCI address, data, byte enable, and command type information, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component”

The Court should adopt Defendants’ proposed construction because it follows the *EMC* construction, which ACQIS agreed to in that case, of the same disputed term and comports with the intrinsic evidence. ACQIS’s proposal attempts to limit a “PCI bus transaction” to a cherry-picked subset of the PCI signals required by the PCI Local Bus Specification, and is contrary to the claim language, patent specifications, and ACQIS’s clear disclaimers before the Patent Office. The *EMC* courts correctly rejected ACQIS’s efforts to disregard the intrinsic record, and this Court should do likewise.

a. “PCI Bus Transaction” Requires a Transaction

The parties dispute whether the claimed “PCI Bus Transaction” is a transaction in accordance with the industry standard PCI Local Bus Specification (Defendants’ proposal), or a mere subset of the information transmitted during a PCI bus transaction (ACQIS’s proposal). Defendants’ proposal is consistent with the plain language of the term, and the intrinsic record, which includes ACQIS’s repeated admissions during *IPR* proceedings that a PCI bus transaction is indeed “a *transaction* according to the protocol set forth in the PCI standard.” Ex. 5 (*EMC Corp. v. ACQIS LLC*, IPR2014-01462, Paper 11 (“873 *IPR* ACQIS Prelim. Resp.”)), at 9.

⁵ See Ex. 26 (Claims Reciting “PCI Bus Transaction”).

First, Defendants’ proposal accords with the unambiguous plain language of the claims. The claims recite a PCI bus **transaction**, not PCI *information*. Although a bus transaction may include the transfer of information, such as address and data information, the intrinsic evidence confirms—as explained below—that a transaction is not limited to just a transfer of information.⁶ ACQIS asks the Court to depart from the plain meaning of the term “transaction” in an apparent attempt to concoct an infringement read. *See Source Vagabond Sys. Ltd.*, 753 F.3d at 1299–1300 (“[A]n ‘analysis’ that adds words to the claim language without support in the intrinsic evidence in order to support a claim of infringement does not follow standard canons of claim construction.”) (internal quotation marks and brackets omitted); *Iris Connex, LLC*, 2016 WL 4596043, at *13 (rejecting proposed construction that was “directed at construing the claim so that it reads on the accused device”).

Second, Defendants’ proposal aligns with what ACQIS told the Patent Office. In its preliminary response to EMC’s *IPR* challenging the ’873 patent, ACQIS repeatedly told the PTAB that a “PCI Bus Transaction is properly limited to bus **transactions** according to the Peripheral Component Interconnect protocol.” Ex. 5 (’873 *IPR* ACQIS Prelim. Resp.), at 5; *id.* at 6 (“The Board similarly should limit . . . ‘PCI bus transaction’ to a bus **transaction** according to that protocol standard.”); *id.* at 9 (“Thus, while the parties’ definitions differ to some extent in the district court, there is no dispute that a PCI bus transaction is a **transaction** according to the protocol set forth in the PCI standard.”). The PTAB agreed with ACQIS, and construed the

⁶ Extrinsic evidence from the time of the purported invention likewise confirms that a bus transaction is more than merely the transfer of information. *See* Ex. 6 (Comprehensive Dictionary of Electrical Engineering, 1998), at 82 (defining bus transaction as “the complete sequence of actions in gaining control of a bus, performing some action, and finally releasing the bus”); Ex. 7 (IEEE The Authoritative Dictionary of IEEE Standard Terms (2 ed. 2000)), at 131 (defining bus transaction as “An event initiated with a connection phase and terminated with a disconnection phase. Data may or may not be transferred during a bus transaction.”).

disputed term as a “Peripheral Component Interconnection (PCI) industry standard bus **transaction**.” Ex. 8 (*EMC Corp. v. ACQIS LLC*, IPR2014-01462, Paper 14 (“‘873 IPR Institution Decision”), at 6-7. Later, at the IPR hearing, ACQIS argued that the PTAB’s construction was correct because the claims “**require a PCI transaction to take place. You are looking at the standard the whole time.** I’m putting a **transaction** together that looks like a PCI transaction.” Ex. 4, (IPR Hr’g Tr.), at 41:23-43:2; 46:14-22.

ACQIS’s definitive statements that a PCI bus transaction is a transaction (and not what ACQIS now claims it to be, just a subset of the information within a transaction) amount to a clear and unmistakable disclaimer of its current assertion that a PCI bus transaction does not include a transaction. *Aylus Networks*, 856 F.3d at 1361 (“[S]tatements made by a patent owner during an IPR proceeding can be considered during claim construction and relied upon to support a finding of prosecution disclaimer.”). ACQIS cannot now credibly argue that a **transaction** is not required when it argued precisely the opposite at the PTAB to preserve patent validity. *Id.* at 1362 (“Extending the prosecution disclaimer doctrine to IPR proceedings will ensure that claims are not argued one way in order to maintain their patentability and in a different way against accused infringers.”).

Third, Defendants’ proposal aligns with what ACQIS told the Massachusetts court. Following ACQIS’s successful defense of the *EMC* IPR challenges, Judge Burroughs held further claim construction proceedings to consider “whether and how IPRs that took place after Judge Davis’s claim construction order should impact this Court’s interpretation.” *EMC D. Mass. Markman*, 2017 WL 6211051, at *2. During those proceedings, ACQIS shifted its position and asked the court to construe the term “PCI bus transaction” as “**information**, in accordance with the PCI Standard, for communicating with an interconnected peripheral component.” Ex. 9 (ACQIS,

LLC v. EMC Corp., No. 14-cv-13560, Dkt. No. 189 (ACQIS Responsive Brief)) at 15. Although ACQIS suggested “information” was interchangeable with “transaction” (*id.* at 17), EMC disagreed and insisted that the construction recite “transaction,” and not mere “information.” EMC explained the term “transaction” was necessary to prevent ACQIS from later seeking to prove infringement by identifying information resembling parts of a PCI bus transaction, as opposed to an actual PCI bus transaction:

The reason . . . this is so important to us is we don’t want there to be any mischief played later on. If they agree that the information that they’re talking about is the transaction as defined in the standard, we’re fine, and that needs to be in the construction. ***What we don’t want is a construction that has this loosey-goosey information language and then have them start to point to things in our products that is not a PCI bus transaction because we don’t do PCI bus transactions in our product.*** We don’t want them to point to that and say, well, that’s information, and here’s how it might relate to the standard in some way. ***Everybody agrees what we’re talking about is something very specific that’s defined in this document.*** . . . The jury should be told that when we’re talking about a PCI bus transaction, we’re talking about a very specific thing that is defined in this industry standard, and it is a transaction.

Ex. 10 (*ACQIS LLC v. EMC Corp.*, No. 1:14-cv-13560, Dkt. No. 350 (“*EMC Claim Construction H’rg Tr.*”)) at 64:19–65:15. Even after EMC clearly distinguished a “transaction” from mere “information,” ACQIS agreed to a construction that recited “transaction.” *Id.* at 167:9–16; *EMC D. Mass. Markman*, 2017 WL 6211051, at *3.

Thus, during the *EMC IPR* and later district court proceedings, ACQIS took the position that a PCI bus transaction is a ***transaction*** in accordance with the PCI Local Bus Specification. The PTAB and district court agreed. This Court should hold ACQIS to its unequivocal past statements, including at the PTAB, and construe the term “PCI bus transaction” as requiring “a transaction.” *Aylus Networks*, 856 F.3d at 1361.

b. A PCI Bus Transaction Requires More than ACQIS’s Cherry-Picked Subset of Information

Beyond omitting the claimed “transaction,” ACQIS’s construction is also wrong because a PCI bus transaction requires more than the particular subset of information ACQIS identifies. As both *EMC* courts found, and the intrinsic evidence confirms, a PCI bus transaction requires more than “PCI address, data, byte enable, and command type information.” Indeed, in the *IPRs* ACQIS distinguished prior art for discarding bits of a PCI bus transaction during communication. Referring to the address, data, and control bits of a PCI bus transaction, ACQIS’s counsel emphasized: “you got to have them all.” Ex. 4 (*IPR* Hr’g Tr.), at 49:12–16; *id.* at 35:13–17, 38:9–17 (ACQIS stated that claims require “the information necessary to make a PCI transaction under the defined standard,” which “*includes the control bits every time.*”).

ACQIS took the opposite position in the *EMC* claim construction proceeding before Judge Davis, and proposed—as it does now—a construction that limited “a PCI bus transaction” to a particular subset of information: “digital command, address, and data information.” *EMC E.D. Tex. Markman*, 2015 WL 1737853 at *4. And ACQIS claimed—as it does now—that the PCI Local Bus Specification supported its proposed construction. *Id.* Judge Davis rejected ACQIS’s attempt to limit a PCI bus transaction to that subset of information, holding that “a PCI bus transaction must include *all* information required by the PCI standard” and “[the PCI Local Bus Specification] *does not clearly define a ‘transaction’ as digital command, address, and data information.*” *Id.* Later, in the claim construction decision following the *IPRs*, Judge Burroughs adopted Judge Davis’ holding that a PCI bus transaction must include “*all* information required by the PCI standard.” *EMC D. Mass. Markman*, 2017 WL 6211051 at *4. As explained below, the intrinsic evidence—including the PCI Local Bus Specification, the asserted patents’ specifications,

and ACQIS's *IPR* statements—shows that the PCI Local Bus Standard does not limit a PCI bus transaction to the subset of information identified by ACQIS.

i. The PCI Local Bus Specification Does Not Limit a PCI Bus Transaction to ACQIS's Subset of Information

The intrinsic evidence confirms a PCI bus transaction is not limited to the four elements ACQIS identifies: “PCI address, data, byte enable, and command type information.” The patents cite the PCI Local Bus Specification as prior art, and expressly reference the “PCI protocols.” *E.g.*, '873 patent at 3:48-54, at 3 (citing “PCI Local Bus Specification (Rev. 2.2., Dec 1998)”). The PCI Local Bus Specification is thus itself intrinsic evidence. *See Kumar v. Ovonic Battery Co.*, 351 F.3d 1364, 1368 (Fed. Cir. 2003) (“[P]rior art cited in a patent or cited in the prosecution history of the patent constitutes intrinsic evidence.”).

The PCI Local Bus Specification demonstrates that a PCI bus transaction requires more than the four elements ACQIS identifies, as it explains that a transaction is an exchange of signals that takes place in a specific sequence and manner. For example, the PCI Local Bus Specification describes a “transaction” as having “[a]n address phase plus one or more data phases.” *See* Ex. 11 (PCI Local Bus Spec.) at 301; *see also id.* at 9 (“A bus transaction consists of an address phase followed by one or more data phases.”). ACQIS's construction ignores that explicit requirement of a PCI transaction. Instead of an address *phase* and a data *phase*, ACQIS's construction requires only “PCI address [and] data . . . *information*.” A phase is not the same as information. A phase is defined as a clock cycle (*i.e.*, a period of time) in which certain signals are sent. *Id.* at 300 (a phase is “one or more clocks in which a single unit of information is transferred”). A POSITA⁷

⁷ Defendants propose a POSITA at the time of the alleged invention would have had at least a Bachelor of Science or equivalent degree in Computer Science or Electrical Engineering, with approximately two years of graduate work, work experience, or the equivalent in computer systems, interfaces, and architecture. Additional graduate education could substitute for

would have understood that a “PCI bus transaction” requires at least what is explicitly defined in the PCI Local Bus Specification—address and data *phases*—and not just any address and data *information*. *Id.* at 301.

Likewise, the PCI Local Bus Specification requires “control signals” as part of a PCI bus transaction. Although ACQIS repeatedly stated during the *IPRs* that the PCI Local Bus Specification requires “control bits,” ACQIS now omits them from its proposed construction. The PCI Local Bus Specification identifies the following as control signals: FRAME#, IRDY#, TRDY#, STOP# (*id.* at 10) and depicts those signals as required, not optional. *Id.* at 7.

Under the heading “Bus Transactions,” the PCI Local Bus Specification describes the sequence of signals, including control signals, required for each specific type of a PCI bus transaction. *Id.* at 46–67. For example, the Specification explains that “a read transaction [] starts with *an address phase which occurs when FRAME# is asserted for the first time[.]*” *Id.* at 47, *see also id.* at 9 (“The address phase is the first clock cycle in which FRAME# is asserted”). The Specification later teaches that the FRAME# control signal also indicates when the read transaction enters its last data phase. *Id.* at 48 (“Only when IRDY# is asserted can FRAME# be deasserted as occurs on clock 8, indicating to the target that this is the last data phase of the transaction.”). In view of these excerpts, a POSITA would have understood that control signals such as FRAME# form a necessary part of the claimed PCI bus transaction.

As another example, the PCI Local Bus Specification describes that each transaction requires a one-bit parity signal to detect errors. *Id.* at 10 (“Parity generation is required by all PCI agents.”), 94 (“Parity on PCI provides a mechanism to determine for each transaction if the master

professional experience, while significant experience in the field might substitute for formal education.

is successful in addressing the desired target and if data transfers correctly between them . . . *During address and data phases, parity covers AD[31::00] and C/BE[3::0]# lines* regardless of whether or not all lines carry meaningful information.”) The PCI Specification explains “[p]arity generation is not optional; it must be done by all PCI-compliant devices.” *Id.* at 94. And yet, ACQIS’s construction excludes parity signals.

ii. The Patent Specifications Do Not Limit a PCI Bus Transaction to ACQIS’s Subset of Information

Consistent with the PCI Bus Local Specification, the patent specifications do not limit a PCI bus transaction to the subset of information ACQIS’s current proposal identifies. For example, the patent specifications disclose that the aforementioned PCI control signals are part of a PCI bus transaction. The specifications include a table (Fig. 16) which shows “the names, types, number of pins dedicated to, and the description of the primary bus PCI signals.” ’873, 22:28–31, Fig. 16. That table lists the control signals FRAME#, IRDY#, and TRDY#, and the specifications elsewhere refer to those signals as control signals. *Id.* at 20:44–47 (“The bits transmitted on lines PD0 to PD3 represent . . . part of the function of *PCI control signals, such as FRAME#, IRDY#, and TRDY#.*”); Fig. 16 (“FRAME# . . . indicates beginning and duration of a PCI transaction.”).

The specifications further state that “[i]n the present invention, *PCI control signals are encoded into control bits and the control bits*, rather than the control signals that they represent, [and] *are transmitted on the interface channel.*” *E.g.*, ’873 patent, 5:33–36. The patents explain that the PCI control signals are converted to “control bits” in order to transmit them on the serial XPBus of the invention. More particularly, the patent specifications describe that an encoder encodes the PCI control signals (including FRAME#) into control bits before a transmitter transmits the control bits on the XPBus interface:

Control encoder & merge data path unit 1025 encodes PCI control signals . . . , merges these encoded control bits and transmits the

merged control bits to transmitter 1030, which then transmits the control bits on the data lines PD0 to PD3 and control line PCN of the XPBus. Examples of control signals include PCI control signals *A specific example of a control signal is FRAME# used in PCI buses.* A control bit, on the other hand is a data bit that represents a control signal.

'873 patent, 17:23–32. Thus, the specifications of the asserted patents confirm that PCI control signals are part of a PCI bus transaction. The Court should reject ACQIS's construction that improperly excludes control signals and other elements required by the PCI Specification.

iii. At IPR, ACQIS Did Not Limit a PCI Bus Transaction to the Subset of Information It Now Identifies

ACQIS's current proposal also contradicts the positions it took during *IPR* proceedings to preserve its patents. For example, during his *IPR* deposition, ACQIS's expert Dr. Lindenstruth unequivocally admitted that a PCI bus transaction requires the control signals that ACQIS now argues are not part of a PCI bus transaction. Counsel for EMC asked Dr. Lindenstruth whether the "*control lines, such as frame [FRAME#], target ready [TRDY#], and so forth*, are [] part of the PCI bus transaction as you understand that term in the claims of the patent?" Ex. 12 (*EMC Corp. v. ACQIS LLC*, IPR2014-01462, Exhibit 1028 ("IPR Dep. Tr. of V. Lindenstruth")), at 145:18–21. Following an objection, counsel rephrased the question and Dr. Lindenstruth answered "yes":

Q. . . . you stated claims require address and data phases of a PCI bus transaction, et cetera. *Are these control lines also part of what the claims require as a PCI bus transaction?*

A. Since they are required to define what is going on on the bus at any point in time, *the answer is yes. They define the PCI transaction.* . . . If you remove any of the flow control signals, you cannot steer the fact if a device is not immediately ready, which happens a lot. *So they would have to be -- they define the transaction, so have to be there.*

Id. at 145:24–146:17.

ACQIS's *IPR* admissions do not end there. ACQIS's counsel also repeatedly told the PTAB that a PCI bus transaction according to the PCI Local Bus Specification requires control bits. For example, counsel told the Board that "control bits" were part of the "information necessary to make a PCI transaction under the defined standard" and "there is no such thing as a PCI transaction that does not have control bits":

That includes the information necessary to make a PCI transaction under the defined standard. That includes data, that includes address except for the interrupt acknowledge, and that includes the control bits every time. So you didn't hear a word about control bits, period. ***There is no such thing -- just put it bluntly, there is no such thing as a PCI transaction that does not have control bits.*** To carve control bits out of claim 54 and 61 is to make sure it does not comply with either the standard of a PCI or the purpose of the invention."

Ex. 4 (*IPR* Hr'g Tr.), at 38:9–17; *see also id.* at 35:11–17 ("[I]f you look at the standard, there are three types of information included in every PCI transaction. Three types. There's an address, there's data and then there's control. That's straight out of the standard. You have those three things.").

In short, ACQIS's current position contradicts its unequivocal admissions during *IPR* proceedings, which ACQIS made to preserve the validity of one of the same patents asserted here. The Court must hold ACQIS to those admissions. *Aylus Networks*, 856 F.3d at 1361.

c. ACQIS's Proposal Attempts to Resurrect Its Rejected Infringement Read, Not Capture How a POSITA Would Have Understood the Intrinsic Record

As demonstrated above, ACQIS's proposal cherry picks only a subset of the information required by the PCI Local Bus Specification and excludes the remaining requirements such as address and data phases, control signals, and parity signals. ACQIS does so because ACQIS cannot dispute that the accused products—which operate according to the newer PCI Express Specification and not the claimed PCI Local Bus Specification—do not have the excluded

requirements of the PCI Local Bus Specification. Indeed, ACQIS admitted as much in the *EMC* litigation with respect to EMC’s products that also operate according to the PCI Express Specification:

EMC contends that, under this claim construction, each of the asserted claims requires a PCI bus transaction in accordance with every element of the Specification, including an address phase followed by one or more data phases as well as control signals and parity signals. . . . ***ACQIS does not dispute that EMC’s products do not include these features.***

EMC D. Mass. Summary Judgment, 2021 WL 1088207 at *4. Based on ACQIS’s admission, Judge Burroughs granted summary judgment of non-infringement. *Id.* The Court should reject ACQIS’s proposal, which omits key requirements of the PCI Local Bus Specification solely for resurrecting ACQIS’s already rejected infringement theory. *Source Vagabond Sys. Ltd.*, 753 F.3d 1291 at 1299–1300; *Iris Connex, LLC*, 2016 WL 4596043, at *13.

d. Collateral Estoppel Bars ACQIS from Relitigating the Construction of “PCI Bus Transaction”

The doctrine of collateral estoppel “precludes a plaintiff from relitigating identical issues by merely ‘switching adversaries’ and prevents a plaintiff from ‘asserting a claim that the plaintiff had previously litigated and lost against another defendant.’” *Phil-Insul Corp. v. Airlite Plastics Co.*, 854 F.3d 1344, 1353 (Fed. Cir. 2017) (quoting *Parklane Hosiery Co. v. Shore*, 439 U.S. 322, 329 (1979)). That is precisely what ACQIS is trying to do—it litigated the same claim construction issues it is now contesting, lost, and switched adversaries to try again. Collateral estoppel applies where, like here: (1) the issue at stake is identical to the one involved in the prior action; (2) the issue was actually litigated in the prior action; and (3) the determination of the issue in the prior action was a part of the judgment in that earlier action. *United States ex rel Gage v. Rolls-Royce N. Am., Inc.*, 760 Fed. App’x 314, 317 (5th Cir. 2019). *See also Phil-Insul Corp.*, 854 F.3d at 1357–58 (affirming finding of collateral estoppel where the district “court correctly concluded that

[plaintiff] was a party in [a previous case], the [disputed] claim terms were construed in [the previous case], construction of those terms was “actually litigated” in that case . . . and the claim constructions were essential to the noninfringement judgments.”). Each requirement is met here.

First, the issue at stake is identical. In *EMC*, the court construed the meaning of “PCI bus transaction,” which is also the disputed term here. Moreover, four of the patents asserted here were also asserted in *EMC*. See Ex. 2 (Family Tree of Asserted Patents). It does not matter that the remaining *patents* differ as long as the issues litigated are the same—*i.e.*, the construction of “PCI bus transaction.” *Ohio Willow Wood Co. v. Alps South, LLC*, 735 F.3d 1333, 1342 (Fed. Cir. 2013) (“Our precedent does not limit collateral estoppel to patent claims that are identical. Rather, it is the identity of the issues that were litigated that determines whether collateral estoppel should apply.”); see also *Sprint Commc’ns Co. L.P. v. Cequel Commc’ns, LLC*, No. 18-cv-1919, 2020 WL 3048175, at *3 (D. Del. June 8, 2020) (applying collateral estoppel where a previous court (1) construed a term of an asserted patent and (2) granted summary judgment based on the construction).

Second, the issue was actually litigated in the *EMC* case. As explained above, ACQIS proposed to Judge Davis a construction equivalent to the one it advances now. And Judge Davis rejected that construction. *EMC E.D. Tex. Markman*, 2015 WL 1737853 at *5 (“[A] PCI bus transaction must include all information required by the PCI standard, ACQIS’s extrinsic evidence does not clearly define a ‘transaction’ as digital command, address, and data information.”). Later Judge Burroughs adopted Judge Davis’ construction (with slight modifications agreed to by ACQIS) and quoted Judge Davis’ critical finding that “a PCI bus transaction must include all information required by the PCI standard.” *EMC D. Mass. Markman*, 2017 WL 6211051 at *4.

Third, the determination of the issue in the prior action was a part of the judgment in that earlier action. Judge Burroughs granted summary judgment of non-infringement on the basis that that the accused products did not contain a PCI bus transaction as construed by the *EMC* courts. *EMC D. Mass. Summary Judgment*, 2021 WL 1088207 at *4 (“All of ACQIS’s arguments are attempts to skirt the claim construction set forth by Judge Davis and this Court.”); *id.* at *5 (“Accordingly, because the accused products do not contain the limitations set forth in the asserted claims, which recite a PCI bus transaction with reference to the Specification, the Court concludes that there is no infringement and summary judgment is appropriate.”). That ACQIS disputes the correctness of Judge Burroughs’s decision is irrelevant. *See Pharmacia & Upjohn Co. v. Mylan Pharms., Inc.*, 170 F.3d 1373, 1380 (Fed. Cir. 1999) (“a district court’s inquiry into whether the plaintiff was afforded a full and fair opportunity to litigate is quite narrow and does not involve a judgment on the merits”). Likewise, the pendency of an appeal does not impact a finding of collateral estoppel. *Id.* at 1381; *Finjan LLC v. SonicWall, Inc.*, No. 17-cv-04467, 2021 WL 3111685, at *3 (N.D. Cal. July 22, 2021) (finding issue preclusion applied and noting the fact that the prior summary judgement order was currently being appealed to the Federal Circuit was a factor *favoring* a finding that the prior order was final and should have preclusive effect).

The three requirements of collateral estoppel are met. Therefore, the Court should preclude ACQIS from advancing its new construction and adopt the *EMC* courts’ construction.

2. Claims Reciting Specific “Bits” of a PCI Bus Transaction, Including But Not Limited to “Address Bits,” “Data Bits,” and “Byte Enabled Information Bits”⁸

⁸ See Ex. 13 (Claims Reciting Specific “Bits” of a PCI Bus Transaction).

Defendants Construction	ACQIS Constructions
“a PCI bus transaction, including all address, data, and control bits”	<p>No construction needed.</p> <p>These phrases recite the bits of a PCI bus transaction that are conveyed / transmitted / communicated, <i>i.e.</i>, “address bits,” “data bits,” and “byte enable information bits,” as applicable. Claims that recite these bits do not require that other, non-recited bits be conveyed / transmitted / communicated. The claims, as written, are clear, and this language of the claims does not require construction.</p>

The Court should adopt Defendants’ proposed construction for two reasons. *First*, Defendants’ construction is correct because it comports with the plain language of the claims. The claims recite specific bits “*of a PCI bus transaction.*” There can be no specific bits of a PCI bus transaction without an actual “PCI bus transaction.” And, as explained above, a PCI bus transaction requires more than address and data bits. ACQIS seeks to read the language “of a PCI bus transaction” out of the claims because it cannot dispute that the accused products do not have PCI bus transactions. The Court should reject ACQIS’s infringement-driven position.

Second, Defendants’ construction is correct because it accounts for ACQIS’s clear and unmistakable disclaimer at *IPR*. As detailed above, at *IPR* ACQIS disclaimed anything less than a full PCI bus transaction. Critically, ACQIS did so for claims that recite conveying a PCI bus transaction *and* for claims—like those here—*that recite conveying specific bits of a PCI bus transaction*. Whether the claims reference specific bits or not, ACQIS’s repeated statements to the PTAB expressly disclaimed the broad construction ACQIS now seeks. The Court should therefore adopt Defendants’ construction.

To preserve the validity of one of the same patents it asserts now, ACQIS’s counsel repeatedly told the PTAB that to comply with the PCI Local Bus Specification, all portions of the PCI bus transaction needed to be transmitted, including the control bits:

- “[I]f you look at the standard, there are three types of information included in every PCI transaction. Three types. There’s an address, there’s data and ***then there’s control***. That’s straight out of the standard. ***You have those three things***.” Ex. 4 (*IPR Hr’g Tr.*), at 35:13–17.
- “[Claim] Fifty-four requires the encoded serial bit stream of peripheral component Internet [sic] connect bus transaction. That includes the information necessary to make a PCI transaction under the defined standard. That includes data, that includes address except for the interrupt acknowledge, and ***that includes the control bits every time***. So you didn’t hear a word about control bits, period. ***There is no such thing -- just put it bluntly, there is no such thing as a PCI transaction that does not have control bits. To carve control bits out of claim 54 and 61 is to make sure it does not comply with either the standard of a PCI or the purpose of the invention***.” *Id.* at 38:7–17.
- So when we talk about [claim] 54, ***you have to talk about control bits***. And not once do they talk about Horst or Bogaerts transmitting ***any type of control bits***. Just doesn’t happen.” *Id.* at 38:18–20
- “[C]laim 54 requires a PCI transaction. ***Got to have control bits***.” *Id.* at 49:13–14.
- “[W]hat that claim requires is that it is a PCI bus transaction. That is defined by the standard. ***You know the three portions: Address, data and control***.” *Id.* at 50:14–16.

Likewise, ACQIS’s *IPR* expert explained that the control bits “define the transaction” and “have to be there.” Ex. 12, at 145:18–146:17. ACQIS’s “repeated and unqualified statements” mean “the interested public is entitled to conclude that the claimed devices and methods” of the patents require that a PCI bus transaction must include all the portions required by the PCI Local Bus Specification, including control bits. *See, e.g., Gammino v. Sprint Commc’ns Co., L.P.*, 577 F. App’x 982, 989 (Fed. Cir. 2014).

ACQIS cannot escape its clear and unmistakable disclaimers, even for the claims that recite “address and data” bits of a PCI bus transaction, because ACQIS made the above disclaimers in the context of claim language that specifically recited “address and data bits.” The *EMC IPR* proceedings involved claims 54 and 61 of the ’873 patent. Claim 54—also asserted here—recites “an encoded serial bit stream of Peripheral Component Interconnect (PCI),” with no reference to specific bits. ’873 patent, 43:40–51. Claim 61, however, recites “wherein the encoded serial bit

stream of PCI bus transaction [of claim 54] comprises encoded *PCI address and data bits*.” *Id.* at 44:5–7. ACQIS’s counsel and expert repeatedly declared that a PCI bus transaction requires control bits despite one of the claims at issue reciting only address and data bits. Therefore, ACQIS’s disclaimer applies equally to the claims here that recite specific bits of a PCI bus transaction.

Moreover, that claim 61 recited specific bits of a PCI bus transaction—while other claims did not—was a central issue in dispute at the *IPR*. *EMC’s counsel* argued that the doctrine of claim differentiation meant that the scope of the PCI bus transaction of claims 54 and 61 were different because claim 61 recited “address and data bits” while claim 54 did not. Ex. 4 (*IPR* Hr’g Tr.), at 14:20–21 (“*So claim 54 has got to be broader than claim 61* and covers a bit stream that’s not even address or data bits.”); 19:22–20:3. But, *ACQIS’s counsel* forcefully opposed EMC’s claim differentiation argument regarding claim 61:

And *an important thing here about [claim] 61*, they said [claim] 61 somehow offers claim differentiation. This is something their expert came up with. Well, if you look at the standard, there are three types of information included in every PCI transaction. Three types. *There’s an address, there’s data and then there’s control. That’s straight out of the standard. You have those three things.*

Id. at 35:11–17. ACQIS’s counsel then explained that the only difference between the “PCI bus transaction” of claim 54 and the “address and data bits of a PCI bus transaction” of claim 61 was that claim 61 carved out “interrupt acknowledgements”:

There is a special type of PCI transaction known as interrupt acknowledge. In an interrupt acknowledge, the address is zeroed out. It’s null. So if you look at claim 54, it says all PCI bus transactions. That covers everything. *What does claim 61 do? Claim 61 narrows it and says this PCI transaction has to have encoded PCI address and data bits. Claim 61 actually carves out those interrupt acknowledges. It carves out a specific type.*

Id. at 35:18–24. Finally, ACQIS’s counsel explained that “*to carve control bits out of claim 54 and 61* is to make sure it does not comply with either the standard of a PCI or the purpose of the invention.” *Id.* at 38:9–17.

Likewise, ACQIS’s *IPR* expert Dr. Lindenstruth stated that claims that recite only specific bits of a PCI bus transaction *still* require transmission of an entire PCI bus transaction, including control signals. At deposition, EMC’s counsel asked Dr. Lindenstruth whether a claim that recited “*address and data bits of PCI transaction* in serial form” required the non-recited “command information.” Ex. 12 (*IPR* Dep. Tr. Of V. Lindenstruth), at 121:5–8. In response, Dr. Lindenstruth explained that despite “explicitly” reciting only “address and data bits,” the claim still requires any “other corollary information which is needed to define a PCI transaction.” *Id.* at 121:13–17 (“It doesn’t say explicitly the other corollary information which is needed to *define a PCI transaction*, but it says “PCI transaction”. So without, for instance, the additional functionality, *it wouldn’t be a PCI transaction.*”). Later, Dr. Lindenstruth clarified that the PCI control lines (like the aforementioned *FRAME#*) were also “corollary signals which basically define what’s going on[.]” *Id.* at 142:17–143:8; *see also id.* at 145:18–146:17 (stating control lines “define the PCI transaction, so have to be there”).

Therefore, ACQIS’s *IPR* counsel and expert unequivocally admitted at *IPR* that claims that recite only specific bits of a PCI bus transaction still require “a PCI bus transaction, including all address, data, and control bits” (Defendants’ proposed construction). The Court must hold ACQIS to those admissions. *Aylus Networks*, 856 F.3d at 1361.

Finally, ACQIS is collaterally estopped from advancing its construction for the same reasons as set forth in Section (III)(B)(1)(d) *supra*. *First*, the issue at stake is identical. In the *EMC* case, the parties asked the court to construe claim terms that were grouped under a

“communicating . . . PCI bus transaction” claim term category which included the claim language “communicate address and data bits of PCI bus transaction.” *See* Ex. 14 (*ACQIS, LLC v. EMC Corp.*, No. 14-cv-13560, Dkt. No. 185 (EMC Opening Brief)) at 21. Consistent with its statements to the PTAB, and notwithstanding that the claim does not explicitly recite control bits, ACQIS agreed that the claim language should be construed as “communicating a PCI bus transaction, *including all address, data, and control bits.*” *EMC D. Mass. Markman*, 2017 WL 6211051, at *8. Importantly, the *EMC* court did not blindly adopt that construction; it made an independent finding that Defendants’ proposed construction was supported by the intrinsic record. *Id.* (“Because this construction is also supported by the intrinsic evidence”). *Third*, the determination of the issue in the prior action was a part of the judgment. The *EMC* court ruled against ACQIS and granted summary judgement of non-infringement by applying the construction the Defendants advance now. *EMC D. Mass. Summary Judgment*, 2021 WL 1088207, at *1. Therefore, ACQIS should be estopped from arguing for a different construction in this case.

3. Claims Reciting an “Encoded” PCI Bus Transaction or a PCI Bus Transaction in “Serial Stream” or “Serial Form”⁹

Defendants Construction	ACQIS Constructions
“a PCI bus transaction that is serialized from a parallel form”	<p>“encoded...”: Code representing a PCI bus transaction</p> <p>Claims reciting a “encoded” PCI bus transaction or PCI bus transaction in “serial stream” or “serial form” (proposed by Defendants): “PCI bus transaction in a serial form”</p>

ACQIS’s unambiguous disclaimers at the PTAB, and the disclosures of the patent specifications, support Defendants’ construction. Despite its prior admission that “one key to the invention was to serialize the otherwise parallel PCI bus transactions,” ACQIS’s construction

⁹ *See* Ex. 15 (Claims Reciting “Encoded” PCI Bus Transactions).

ignores the parallel form of PCI bus transactions—the very reason the patents’ specifications consistently disclose that transactions must be “encoded” for transfer via a serial interface. The *EMC* court effectively adopted Defendants’ proposed construction¹⁰ for the same and similar terms¹¹ in view of the same record, and there is no sound reason for this Court to adopt a different construction.

a. As the *EMC* Court Found, ACQIS’s Numerous and Repetitive Statements in the *IPRs* Show that an Encoded PCI Bus Transaction Requires that a PCI Bus Transaction Is Encoded from Parallel to Serial Form

To preserve the validity of its patents during the *EMC IPRs*, ACQIS made clear and unambiguous statements that its patent claims require taking PCI bus transactions in their original parallel form, converting to serial form, and then back to parallel form. The Court should adopt Defendants’ proposed construction in view of ACQIS’s disclaimer.

First, in its *IPR* papers, ACQIS argued “[a]s described in the specification . . . *one key to the invention was to serialize the otherwise parallel PCI bus transactions* to increase communication speeds for peripherals.” Ex. 3 (’873 *IPR* ACQIS Resp.) at 3. ACQIS distinguished the prior art from the ’873 patent (also asserted here) on the basis that the prior art did not perform this “key” serialization. *Id.* at 21–22 (“Horst never serializes any PCI bus transaction; even the peripheral-side PCI bus transaction . . . Horst teaches a different architecture and never serializes an actual PCI bus transaction.”).

¹⁰ Defendants’ proposal modifies the verb tense of the *EMC* Court’s construction from “has been” to “is.”

¹¹ The claim terms in *EMC* were: “encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction” (’873 Patent, claims 6, 54 (also asserted here), 65); “serial channels that transmit encoded data of Peripheral Component Interconnect (PCI) bus transaction” (’814 Patent, claim 24); and “an encoded serial bit stream . . . of [a] Peripheral Component Interconnect (“PCI”) bus transaction” (’468 Patent, claim 29). *See* Ex. 14 (EMC Op. Cl. Constr. Br.) at 15. The court identified these terms as “encoded . . . serial bit stream of Peripheral Component Interconnect (PCI) bus transaction” and related terms. *EMC D. Mass. Markman*, 2017 WL 6211051 at *5.

Second, during oral argument before the PTAB, ACQIS’s counsel explained that ACQIS’s invention is like an “**hourglass**” in which the PCI transaction in its original parallel form is converted (or encoded) to serial form for transmission over serial channels, and then converted (or decoded) back to parallel form for compatibility with the PCI protocol. ACQIS’s counsel’s statements were clear and unmistakable. *E.g.*, Ex. 4 (*IPR Hr’g Tr.*), at 39:21–40:2 (“You have got a standard PCI bus, you have got the invention, depending on how you do it, but ***you have got the new bus in the center, and what that’s doing is taking the parallel 32 bits coming down, putting them on a serial bus, moving them and then taking them back out. It’s an hourglass***[.]”), 32:2–4 (“You start with the PCI address that’s in this parallel slow form, serialize it and then take it back to the PCI form at the other end.”), 34:14–18 (“But the whole point of this invention and these claims is that they are centered around dealing with a standard. All of the computers out there have PCI . . . And the point is you take it from parallel to serial and then back to parallel.”), 46:14–47:18 (“So I have created my PCI transaction . . . And then I’m taking it at a parallel form, putting it into serial form and then back to parallel.”); 65:13–23 (“Remember I said the hourglass, you start with the PCI, you got the parallel bits, serialize them, get them to the other side, push them back out.”).

ACQIS’s counsel further emphasized this point in response to a question from the Board about whether the prior art’s disclosure of encoding that did not involve a parallel—serial—parallel conversion was covered by the claims, to which ACQIS responded:

It absolutely doesn’t because you are never starting with an address here. So their expert describes it before he changed his position in his original declarations, he describes it as Scrabble cubes. I’ve got a PCI address, I have got it spelled out here, 32-bit word, and I take it, I put it on my serial line. ***So that’s the whole point. I’m going from parallel, I’m putting on a serial line.*** And on the bottom end I have got to be able to reassemble my word. I have got my rules. I know what to do.

Id. at 30:13–31:2; 51:11–12 (“You have to encode, have the encoded PCI transaction. So it is the hourglass.”).

As the *EMC* court recognized, ACQIS’s repeated, unequivocal statements regarding the scope of its invention requires a construction that accounts for that disclaimer:

ACQIS’s numerous and repetitive statements in the IPRs clearly and unmistakably show that an encoded PCI bus transaction requires that a PCI bus transaction be encoded for serial transmission from a parallel form. Similar to *Aylus*, ACQIS repeatedly represented that “the whole point” of the invention is to convert a PCI bus transaction from parallel to serial and back to parallel. ACQIS’s argument was not only clear and unmistakable but also consistent throughout its briefing and oral argument. Each of the statements identified above reinforced ACQIS’s chosen metaphor of the hourglass, which, if nothing else, represents a PCI bus transaction beginning in parallel, converting to serial, and then back to parallel.

EMC D. Mass. Markman, 2017 WL 6211051 at *7 (internal citations omitted). Accordingly, the *EMC* court construed “encoded . . . serial bit stream of Peripheral Component Interconnect (PCI) bus transaction and related terms” as “a PCI bus transaction that has been serialized from a parallel form.” *Id.* at 8. This Court should likewise find ACQIS’s statements were a disclaimer and adopt the Defendants’ proposed construction.

b. The Patent Specifications Support Defendants’ Construction

ACQIS’s proposal seeks to isolate “encoded” and “serial” in order to argue those claim terms do not require parallel-to-serial conversion. But the specifications uniformly describe that such conversion is necessary. As discussed herein, ACQIS’s alleged invention provides a *serial* interface channel (the XPBus) to communicate parallel PCI transactions converted to serial form. *E.g.*, ’873 patent, at 3:7–10 (“[T]he present invention relates to an interface channel that interfaces two computer interface buses that operate under protocols that are different from that used by the interface channel.”); 5:31–33 (“The present invention overcomes the aforementioned

disadvantages of the prior art by interfacing two PCI or PCI-like buses using a non-PCI or non-PCI-like channel.”); 6:25–48 (discussing serial interface channel); *see also* Ex. 24 (*EMC Corp. v. ACQIS LLC*, IPR2014-01462, Ex. 2021 (*IPR Decl. of V. Lindenstruth*)), ¶ 63 (“The PCI standard bus was a 32-bit wide *parallel* bus[.]”). The specifications detail the parallel—serial—parallel conversion (that is, the “hourglass”).

For example, Figures 7 (or 17) and 8 (or 18) of the asserted patents (shown below) each depict a computing system coupled to a peripheral system through an **interface channel** (outlined in orange), with an “**interface controller**” (outlined in red) at either side of the interface channel:

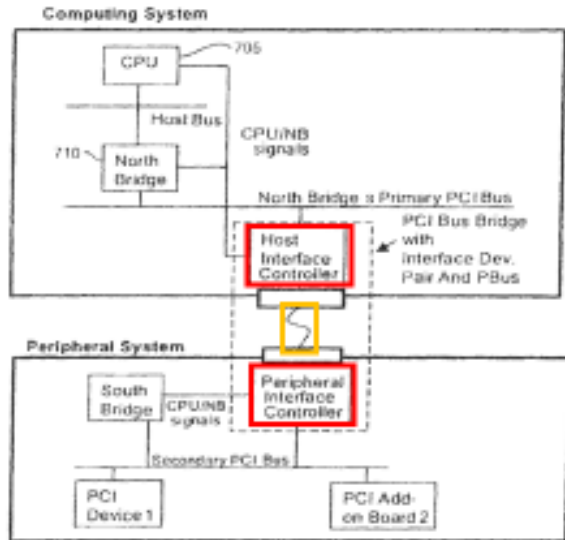


FIGURE 7

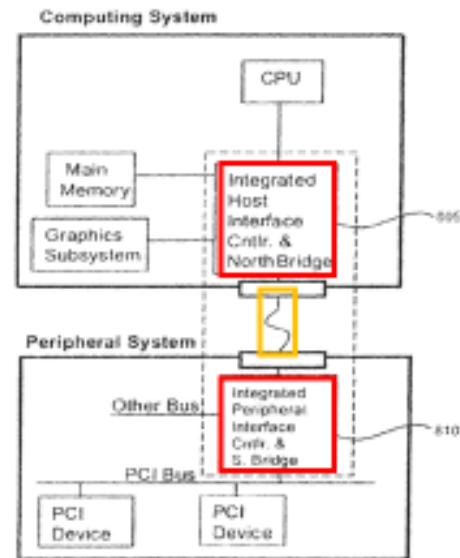


FIGURE 8

’873 patent, Figs. 7 and 8; ’739, Figs. 17 and 18. Figure 10 (or 14) of the asserted patents (shown below) illustrates the connection between an **interface controller** (outlined in red) and a **serial interface** (the XP Bus outlined in orange). The interface controller contains **parallel to serial converters** (shown in blue) which convert outbound PCI bus transaction data (from left to right) from parallel to serial form, and **serial to parallel converters** (shown in green) which convert

inbound PCI bus transaction data (from right to left) from serial to parallel. '873 patent, Fig. 10; 16:53–60, 17:41–18:7; '739 patent, Fig. 14.

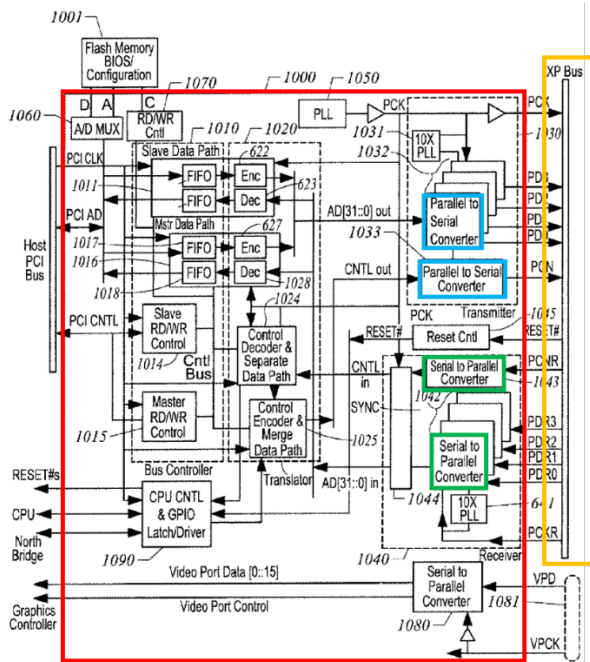


FIGURE 10

Thus, the patents' specifications comport with what ACQIS told the PTAB, that "one key to the invention was to serialize the otherwise parallel PCI bus transactions." Ex. 3 ('873 IPR ACQIS Resp.), at 3.

The specifications further acknowledge that "[i]nterfaces coupling two independent computer buses" were well known, thus, the "present invention relates to an interface channel that interfaces *two computer interface buses that*

operate under protocols that are different from that used by the interface channel." '873 patent, 3:6–12. In other words, parallel PCI bus transactions operate under a different protocol than the serial interface channel of the alleged invention. More specifically, to transmit parallel PCI bus transactions over the serial interface, the specifications explain that the PCI bus transactions are encoded for conversion to serial form, then transmitted over the interface channel. The specification discloses how various elements of the PCI bus transaction—including all PCI address, data and control signals—are encoded for conversion from parallel to serial form. *See, e.g.,* '873 patent, at 5:33–36 ("In the present invention, PCI control signals are encoded into control bits and the control bits, rather than the control signals that they represent, are transmitted on the interface channel."); *id.* at 16:55–58 ("**Encoders 1022 and 1023 format the PCI address/data bits** to a form more suitable for parallel to serial conversion prior to transmittal on the XPBus."); *see*

also id. at 17:8–13 (“encoders 1022 and 1027 . . . encode the PCI address and data information into a form more suitable for parallel to serial conversion prior to transmittal on the XPBus.”); 17:23–28 (“Control encoder & merge data path unit 1025 *encodes PCI control signals . . . into control bits*, . . . then transmits the control bits on the data lines PD0 to PD3 and control line PCN of the XPBus.”). After passing through the serial interface, the serialized form of the PCI transaction is converted for decoding back to a parallel form and decoded for use once again under the PCI protocol. *See, e.g.*, ’873 patent, at 5:36–39 (“At the receiving end, the control bits representing control signals are decoded back into PCI control signals prior to being transmitted to the intended PCI bus.”); *id.* at 16:58–60 (“Similarly, address and data information from the receivers is decoded by decoders 1023 and 1028 to a form more suitable for transmission on the host PCI bus.”); 17:36–40 (“Control decoder & separate data path unit 1024 separates the control bits it receives . . . and decodes the control bits into PCI control signals, . . .”). In short, encoding a PCI bus transaction goes hand in hand with the parallel to serial conversion.

The Court should adopt Defendants’ construction, which accounts for ACQIS’s clear disclaimers about the central purpose of the alleged invention, and the unmistakable teachings of the specification.

C. “Universal Serial Bus (USB) protocol”¹²

Defendants Construction	ACQIS Constructions
“[data/information conveyed according to] the protocols defined in the Universal Serial Bus Specification Revision 2.0 and prior versions of the Universal Serial Bus Specification”	“Universal Serial Bus (USB) protocol” / “Universal Serial Bus (USB) protocol data”: USB data payload “Universal Serial Bus (USB) protocol information”: information described in the USB specification

¹² *See* Ex. 16 (Claims Reciting “Universal Serial Bus (USB) protocol”).

The Court should adopt Defendants’ proposed construction for two reasons. *First*, Defendants’ proposal aligns with the intrinsic evidence and makes clear what ACQIS has already conceded elsewhere: “the term ‘USB’ refers to the versions of the USB specification in existence at the time of the invention, including USB 2.0 and prior versions.” Ex. 17 (*ACQIS LLC v. Samsung*, No. 2:20-cv-00295, Dkt. No. 71 (“ACQIS-Samsung Reply Br.”)), at 10 (August 3, 2021). *Second*, Defendants’ proposal specifies that the USB claim terms are characterized by the protocols defined in the relevant specifications, which is how a POSITA would have understood them. As with the PCI bus transaction term above, ACQIS’s proposal seeks to improperly broaden the claims to cover after-arising technology by requiring only a subset of the information described in the claimed protocol specifications.

1. In the Patents, “USB” Refers to the USB 2.0 Specification and Prior Versions, a Fact that ACQIS Conceded Elsewhere

“The ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question *at the time of the invention*, *i.e.*, as of the effective filing date of the patent application.” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005). Here, at the purported effective filing dates of the Patents-in-Suit—May 14, 1999 and May 12, 2000—the latest version of the Universal Serial Bus Specification in existence was Revision 2.0 (the “USB 2.0 Specification”). Ex. 20 (USB Spec. 2.0) at 1 (dated April 27, 2000). The Non-Reissue Asserted Patents explicitly refer to the USB 2.0 Specification. *E.g.*, ’873 patent, 11:28–31 (“For example, the invention can use Gbit Ethernet 1394, and **USB 2.0**.”), 11:40–42 (“The implementation is not restricted to Ethernet serial communication and can use other high-speed serial communication such as **USB 2.0**, and 1394.”). A POSITA would have understood that when the claims recite “Universal Serial Bus (USB) protocol,” they are referring to the protocols defined in the USB 2.0 Specification and prior versions, and not later versions of the

USB specification not yet in existence. *See Fundamental Innovation Sys. Int’l LLC v. Samsung Elecs. Co.*, No. 2:17-cv-145, 2018 WL 647734, at *11 (E.D. Tex. Jan. 31, 2018) (“[T]he term ‘USB’ in the patents-in-suit should be limited to the Universal Serial Bus standards that existed at the time of the claimed invention.”); *Extreme Networks, Inc. v. Enterasys Networks, Inc.*, No. 07-cv-229, 2007 WL 5601497, at *17 (W.D. Wis. Nov. 21, 2007) (“An invention cannot comply with standards not yet in existence. Defendant argues that limiting the standards to a particular version could render the invention obsolete as the standards change. Defendant is correct, but that is not an argument for expanding the reach of a claim beyond what could have been anticipated by the inventor; it is an argument for not including as an element in a claim a set of standards that change over time.”).

ACQIS (and its expert Dr. Levitt) conceded in the parallel *Samsung* litigation that the claimed USB terms refer to the USB 2.0 Specification and prior versions. Ex. 17 (ACQIS-Samsung Reply Br.) at 10 (August 3, 2021) (“[T]he term ‘USB’ refers to the versions of the USB specification in existence at the time of the invention, including USB 2.0 and prior versions.”); Ex. 18 (Dep. Tr. of M. Levitt (June 23, 2021) at 43:9–18 (“[W]ithin the patents and what is mentioned in the time frame, it is – it would be the appropriate parts of USB 2.0 or potentially earlier versions, which would be 1.1.”). In view of those concessions, ACQIS cannot credibly oppose Defendants’ construction, which tracks what a POSITA would have understood at the time of the invention. And yet ACQIS proposes a construction untethered to the patent disclosure in order to read its claims on accused products that use *the later USB 3.0* specification. *E.g.*, Ex. 19 (ACQIS’s Infringement Contentions Against Lenovo Defendants, Appendix F), at 3 (“Plaintiff identifies *USB 3.0 and later* communication channels and related hardware throughout Appendix F as satisfying the foregoing claim limitations . . . The ThinkSystem SR670 has one or more *USB 3.0*

or later ports.”). The Court should adopt Defendants’ proposal that “Universal Serial Bus (USB) protocol” refers to “the protocols defined in the Universal Serial Bus Specification Revision 2.0 and prior versions of the Universal Serial Bus Specification.”

2. The USB Claim Terms Are Not Limited to ACQIS’s Subset of Information

Because ACQIS knows that the claims refer only to the USB 2.0 and earlier specifications, ACQIS’s proposed construction requires only a subset of information from the outdated standards that ACQIS contends is also in the modern standards. However, as explained, a POSITA would have looked to the USB 2.0 Specification—which is intrinsic evidence on the face of the asserted patents—to understand what was required for the recited USB terms.

a. “USB Protocol Data Packets” Are More than “USB Data Payloads”

Eight of the asserted claims recite “Universal Serial Bus (USB) protocol data packets”¹³ or “data packets in accordance with a Universal Serial Bus (USB) protocol.”¹⁴ ACQIS proposes that the Court construe those terms as merely “USB data payload.” ACQIS’s construction is wrong because the relevant USB specifications teach that a USB data packet is more than a data payload. For example, the USB Specification 2.0 explains, under the heading “8.4.4 Data Packets,” that “[a] data packet consists of a PID, a data field containing zero or more bytes of data, and a CRC as shown in Figure 8-15.” Ex. 20 (USB Spec. 2.0) at 206; Figure 8-15 (annotations added):

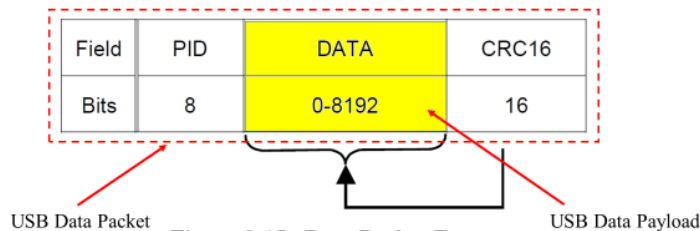


Figure 8-15. Data Packet Format

¹³ '750 patent, claims 4, 7, 24, 46.

¹⁴ '359 patent, claims 1, 6, 19; '977 patent, claim 1.

Figure 8-15 above shows that ACQIS's proposed information, the data payload highlighted in yellow, is but one element of the USB data packet, outlined in red. Adopting ACQIS's proposal would exclude the other requirements of a USB data packet: an 8 bit packet identifier value (PID) and a 16 bit cyclic redundancy check (CRC) value. Those other elements are not optional—a USB data packet must comply with the protocols specified in the USB specification, or it would cease to be a USB data packet. *See, e.g., id.* at 8 (defining PID as a “field in a USB packet that indicates the type of packet, and by inference, the format of the packet and the type of error detection applied to the packet.”). In other words, a POSITA would have understood at the time of the invention that a USB data packet required all of the “protocols defined in the Universal Serial Bus Specification Revision 2.0 and prior versions of the Universal Serial Bus Specification” (Defendants' proposal), such as the 8 bit PID and 16 bit CRC, and not just a USB data payload.

ACQIS cannot credibly contend that a USB data packet is the same as a USB data payload. In the *Samsung* litigation, ACQIS's expert Dr. Levitt testified that a USB data packet “*includes* a USB data payload,” not that a USB data packet *is* a USB data payload. Ex. 21 (Decl. of M. Levitt), ¶ 139. Furthermore, adopting ACQIS's proposed “USB data payload” construction would render the recited USB claim terms meaningless. As Dr. Levitt explained, the USB data payload is a collection of bytes with no real format or requirements:

[T]he data payload is the field within the data packet that holds data. And data for within USB is just a collection of bytes that specifically has no real format or – or exact meaning with there . . . USB does not impose really any specific meaning to the data payload or data fields.

Ex. 18 (Dep. Tr. of M. Levitt), at 42:11–19. Thus, ACQIS's proposal would read the claimed USB protocol out of the claim language and impermissibly broaden it to cover *any* “collection of bytes.”

b. “USB Protocol Data/Signals” Are also More than “USB Data Payloads”

Fifteen of the asserted claims recite “Universal Serial Bus (USB) protocol data,”¹⁵ “Universal Serial Bus (USB) protocol signals,”¹⁶ conveying data using a “Universal Serial Bus (USB) protocol,”¹⁷ or “utilizing a Universal Serial Bus (USB) protocol”¹⁸ (collectively, the “USB Protocol Data Terms”). ACQIS’s proposal would reduce all of the USB Protocol Data Terms to merely the USB data payload. However, as explained above, a USB data payload is just one part of a USB data packet. And USB data packets are just one form of USB protocol data or signals—the USB 2.0 Specification requires more than the transmission of data packets or data payloads to implement the USB protocol. Indeed, the USB 2.0 Specification defines a “protocol” as a “specific set of rules, procedures, or conventions relating to format and timing of data transmission between two devices.” Ex. 20 (USB 2.0 Spec.) at 8. As one of those “specific set of rules,” the Specification explains that USB 2.0 transactions require three elements: a “token packet,” a “handshake packet,” and a “data packet.” *Id.* at 18–19. A POSITA would have understood the USB Protocol Data Terms to require USB 2.0-compliant transactions, not just the transmission of USB data payloads, which ACQIS has admitted are “just a collection of bytes” with “no real format.” Ex. 18 (Dep. Tr. of M. Levitt), at 42:11–19.

c. “USB Protocol Information” Refers to the USB 2.0 Specification and Earlier Versions

Finally, claim 14 of the ’947 patent recites “Universal Serial Bus (USB) Protocol Information.” ACQIS proposes the Court should construe that term as “information described in

¹⁵ ’359 patent, claim 17; ’654 patent, claims 20, 23; ’739 patent, claims 14, 18, 30; ’769 patent, claim 19; 468 patent, claim 21.

¹⁶ ’977 patent, claims 11, 17.

¹⁷ ’750 patent, claims 48, 50; ’768 patent, claims 36, 40.

¹⁸ ’768 patent, claim 34.

the USB specification.” ACQIS’s construction is wrong because it does not limit the information to the USB 2.0 and earlier specifications, which ACQIS admitted the claims reference. Ex. 17 (ACQIS-Samsung Reply Br.) at 10 (“[T]he term ‘USB’ refers to the versions of the USB specification in existence at the time of the invention, including USB 2.0 and prior versions.”). Therefore, the Court should adopt Defendants’ proposal, which identifies the indisputably correct USB specifications: “information conveyed according to the protocols defined in the Universal Serial Bus Specification Revision 2.0 and prior versions of the Universal Serial Bus Specification.”

D. “Computer Module”¹⁹

Defendants Construction	ACQIS Construction
“a user-removable, user-portable computer system within an enclosure comprising at least a processor, memory, and mass storage”	“A computing package for providing a computing function as recited in a particular claim.”

The parties agree that “computer module” is not a term of art in the industry, and thus propose competing constructions. Defendants’ construction should be adopted because it clarifies the scope of the relevant claim terms and aligns with the specifications of the Asserted Patents. In contrast, ACQIS’s proposal is untethered to the intrinsic evidence and could apply to any component of any computer system.

The intrinsic record is clear that the claimed “computer modules” within the modular computer system are substantially similar to one another and capable of “independent processing.” ’768 patent, abstract; *see also id.* at 1:39-43, 4:17-29, 38-59. Consistent with Defendants’ proposal, the specifications of the Asserted Patents repeatedly state that the claimed “computer module”—in every embodiment described in the specifications—consists of an “*enclosure* that is

¹⁹ ’873 patent, claims 54, 77; ’624 patent, claims 6, 11; ’602 patent, claim 14; ’984 patent, claims 40, 52.

insertable into a console,” and which houses the components required for device protection and security purposes. ’768 patent, 7:7-13, 29-32, 9:61-62, 10:27-34, 29:60-67, 36:1-16 & Figs. 1, 19, 19B, 24; ’654 patent, 7:61-67, 9:32-35 & Figs. 1-2.

The specifications further explain that the “enclosure” of the computer module contains at least “a processing unit, a main memory coupled to the processing unit, ... and a mass storage device coupled to the processing unit.” ’768 patent, at 4:17-20; *see also id.* at 4:38-41, 4:52-57. 9:55-58, 10:27-42; 26:35-39, 35:35-39, 35:45-50; 36:1-16; ’654 patent 5:53-56, 7:61-67, 10:41-67 & Fig. 5. The mass storage unit would contain the operating system, application software and data. ’768 patent 37:15-17; ’654 patent 7:22-24. This configuration facilitates (i) user operation of multiple computer modules in the modular computer system, and/or (ii) multiple users sharing the same modular computer system but independently operating one or more of the computer modules. ’768 patent, 5:7-16; ’654 patent, 9:66-10:20.

In addition, the claimed computer modules require user portability and avoid the drawbacks of conventional portable computers, such as laptops. *See* ’768 patent, 2:14-55; ’654 patent, 2:6-46. According to the patents, laptops at the time of the invention lacked the usability and power of a desktop computer but were nonetheless necessary because desktop computers were not portable—*i.e.*, they were not fit for use “on the road.” ’768 patent 2:14-3:17; ’654 patent 2:6-3:5. The patents teach that the claimed invention addresses this issue by incorporating the core computing components—CPU, memory, storage—into a portable enclosure configured for insertion into a module bay of a peripheral console. ’654 patent 5:41-2:30 & Fig. 2; ’768 patent 30:62-32:7 & Figs. 19b-20. A stated advantage of this alleged inventive “computer module” is that its “[i]nclusion of high cost, high performance components . . . concentrates a user’s core computing power and environment in a **portable** package.” ’768 patent 28:66-29:3.

The patents teach that an important aspect of the portability of the module is that a user can easily insert it into and remove it from a module bay in a console. '768 patent 7:24-29, 9:50-54, 10:3-14 & Fig. 1; '654 patent 3:58-60, 5:46-52, 6:24-30 & Figs. 1-2. For example, the reissue patents state that the "computer module" is "a **removable** module with memory and microprocessor." '654 patent 3:59. In fact, many of the alleged inventive embodiments described in the patents are directed to supporting this user-removability. For example, the patents describe embodiments to prevent users' accidental removal of the computer module(s) from the modular computer system and/or access by unauthorized users during transit. '768 patent, 7:49-52; '654 patent, 4:34-40. Indeed, the specification of the Reissue Asserted Patents specifically describes methods for identifying users by initiating a security program that requires users to enter credentials for accessing the modular computer system when a computer module is first inserted into it. *See, e.g.*, '654 patent, 3:66-4:3, 4:10-20.

While ACQIS will undoubtedly try to underplay the importance that the specifications place on the removability and portability of the computer module, ACQIS was forced to admit this clear disclosure when questioned by Judge Davis during the *Markman* hearing in the *EMC* case. Ex. 25 (*ACQIS LLC v. Alcatel-Lucent USA Inc., et al.*, No. 6:13-cv-638, Dkt. No. 175), at 49:7–12 ("THE COURT: But your whole patent and specification envisions a removable module, doesn't it? I mean, for the -- for it to be used from one to another? MR. SAUER: Yes, Your Honor. . . That's correct.").

Defendants' proposed construction captures the Asserted Patents' repeatedly disclosed feature of user portability of the computer module, as well as the essential elements required for independent processing. On the other hand, Plaintiff's construction does not derive from the intrinsic record and provides no bounds or guidance as to the appropriate scope of the claim term.

See U.S. Surgical Corp. v. Ethicon, Inc., 103 F.3d 1554, 1568 (Fed. Cir. 1997) (“Claim construction is a matter of resolution of disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims[.]”). There is no reference anywhere in the specifications—and certainly not in connection with the term “computer module”—to a “computing package” or a “computing function,” or what those terms mean, particularly in view of ACQIS’s added phrase “as recited in a particular claim.” ACQIS’s proposed construction has no support in the intrinsic record, and would serve only to confuse the jury. Defendants’ construction should therefore be adopted because it clarifies the scope of the claim term and is fully consistent with the specifications of the Asserted Patents.

E. “Console”²⁰

Defendants Construction	ACQIS Construction
“enclosure, housing at least one bay for receiving a computer module, which connects components of a computer system”	“A device or enclosure, housing one or more coupling sites, that connects components of a computer system.”

The parties’ dispute regarding the claimed “console” revolves around (i) whether the console houses “one or more coupling sites” (ACQIS’s construction) or “at least one bay for receiving a computer module” (Defendants’ construction) for connecting the components of the modular computer system, and (ii) whether the console can be properly construed as *any* “device” that connects components of a computer system.

As to the first dispute, Defendants’ proposed construction should be adopted because all of the embodiments of the claimed “console” described in the patent specifications contain at least one “computer module bay” so that a “computer module” can be inserted into the “console” in

²⁰ ’768 patent, claims 18, 22, 30, 34; ’750 patent, claims 5, 10, 18, 24, 35, 44, 48; ’873 patent, claims 54, 77; ’624 patent, claims 6, 11; ’359 patent, claims 1, 4, 6, 8, 17, 19-21; ’977 patent, claims 1, 4; ’654 patent, claims 14, 23; ’468 patent, claims 26, 29; ’739 patent, claim 18; ’602 patent, claim 14; ’984 patent, claim 40; ’140 patent, claims 14, 31.

order “to form a functional computer.” *See* ’768 patent 7:3-6, 9:55-64, 10:4-6; 10:57-11:8, 14:63-15:1, 29:60-30:22, 30:62-31:27, 37:34-55, 39:40-49 & Figs. 1, 19, 19B; ’654 patent 3:43-49, 5:56-62, 6:22-30, 8:7-21 & Fig. 1. The specifications also expressly state that a “coupling site” is a “computer module bay.” *See, e.g.*, ’768 patent 4:30-35, 10:3-10.

ACQIS’s proposal should be rejected because the term “coupling site” is not recited anywhere in the specification or claims of the Reissue Asserted Patents, and appears only the “Brief Summary of the Invention” of the Non-Reissue Asserted Patents. *See, e.g.*, ’768 Patent, 4:32-35, 46-50. Not only do the patents provide little guidance, but the term “coupling site” has no plain and ordinary meaning, as the parties appear to agree.

ACQIS’s construction also cannot be correct because the proposed “coupling sites” are not limited to those adapted for receiving a computer module, which is the purpose and function of the console disclosed in the Asserted Patents. Indeed, ACQIS’s proposed “coupling sites” are not bounded by *any* particular structure or function—they could refer to any connection on any device or enclosure for connecting components of a computer system. In contrast, Defendants’ construction properly limits both the structure (to “at least one bay”) and the function (to “receiving a computer module”) associated with the claim term.

Regarding the parties’ second dispute, there is no support for ACQIS’s construction that a “console” can be a “device.” The specification does not use the term “device” anywhere in connection with the term “console.” Instead, the console is described as either a “chassis” (’768 Patent 10:57-58) or an “enclosure” (*id.* at Abstract, 4:49-50).

Therefore, Defendants’ construction should be adopted at least because: (1) the Asserted Patents expressly disclose that the claimed “console” includes one or more computer module bays

adapted for receiving computer modules; (2) ACQIS's construction is unbounded by the intrinsic evidence; and (3) there is no support for ACQIS's construction that a "console" can be a "device."

F. "Single Chip"²¹

Defendants Construction	ACQIS Construction
Plain and ordinary meaning, wherein the plain and ordinary meaning is "one integrated circuit chip"	No construction needed. Plain and ordinary meaning.

Defendants' construction reflects the plain and ordinary meaning of a "single chip." ACQIS disagrees, and apparently holds the view that a "single chip" can include multiple integrated circuit die, *e.g.*, interconnected together on a common semiconductor substrate. ACQIS's apparent position that the scope of the "single chip" claim term encompasses multiple-chip implementations would effectively read out the claim term "single" altogether. Defendants have therefore proposed a construction to resolve this dispute and to clarify the proper scope of the ordinary meaning of the term. *See O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1361 (Fed. Cir. 2008).

Defendants' proposal should be adopted because a POSITA would understand that a single integrated circuit chip is being claimed—not multiple chips. Numerous dictionary definitions at the time of the alleged invention support Defendants' interpretation:

- Modern Dictionary of Electronics' definition of "chip": "2. **A single substrate on which all the active and passive circuit elements have been fabricated** using one or all of the semiconductor techniques . . . 3. **A tiny piece of semiconductor material**, scribed or etched from a semiconductor slice, on which one or more electronic components are formed."²²
- Comprehensive Dictionary of Electrical Engineering's definition of "chip": "(1) a small piece of semiconductor material upon which miniaturized electronic circuits can be built. (2) **an individual MMIC circuit or subsystem** that is one of several

²¹ '768 patent, claims 1, 4, 13, 18, 22, 36, 39; '750 patent, claims 1, 5, 6, 10, 11, 24, 25, 31, 35, 37, 45, 48, 50; '797 patent, claims 36, 38; '359 patent, claim 1; '977 patent, claims 1, 6, 13, 14; '769 patent, claim 19; '739 patent, claims 18, 29; '602 patent, claim 14; '140 patent, claims 14, 30, 35.

²² Ex. 22 (Modern Dictionary of Electronics', Elsevier Science & Technology (1999)), at 113.

identical chips that are produced after dicing up an MMIC wafer.”;²³ and

- Comprehensive Dictionary of Electrical Engineering’s definition of “integrated circuit”: “(1) an assembly of miniature electronic components **simultaneously produced in batch processing, on or within a single substrate**, that performs an electronic circuit function. (2) many transistors, resistors, capacitors, etc., **fabricated and connected together to make a circuit on one monolithic slab of semiconductor material.**”²⁴

For the foregoing reasons, Defendants’ proposal for the ordinary meaning of the term “single chip” should be adopted.

G. “Central Processing Unit”²⁵

Defendants Construction	ACQIS Constructions
Plain and ordinary meaning, wherein the plain and ordinary meaning is “a single central processing unit or core processing unit”	No construction needed. Plain and ordinary meaning.

Defendants’ construction should be adopted because it is consistent with the specifications of the Asserted Patents as understood by a POSITA. At the relevant time, a person of ordinary skill in the art would have understood a CPU to refer to a single processing unit or core as opposed to multiple ones. A construction of “central processing unit” is thus needed to distinguish what constitutes a single CPU from dual-core and multi-core CPUs.

Consistent with Defendants’ proposal, the specification of the Non-Reissue Asserted Patents expressly distinguishes CPU systems from Dual-CPU systems. *See, e.g.*, ’768 patent 2:61-3:17. *See also id.* at Fig. 2 (showing two CPUs connected with a shared peripheral system). Similarly, the specification of the Reissue Asserted Patents specifically identifies a single-CPU

²³ Ex. 23 (Comprehensive Dictionary of Electrical Engineering, CRC Press (1998)), at 110.

²⁴ Ex. 23, at 356.

²⁵ ’768 patent, claims 1, 4, 7, 10, 13, 18, 33, 30, 33, 34, 36, 39; ’750 patent, claims 1, 5, 6, 10, 11, 18, 21, 24, 25, 27, 29, 31, 34, 35, 37, 44, 45, 46, 47, 48, 50; ’797 patent, claims 7, 8, 10, 14, 16, 36; ’359 patent, claims 1, 2, 4, 6, 8, 17, 19; ’977 patent, claims 1, 6, 12, 13, 14; ’769 patent, claim 19; ’654 patent, claims 14, 23; ’468 patent, claims 14, 21, 26, 29, 35, 37, 45; ’947 patent, claims 14, 19, 35, 48, 51, 54, 57; ’739 patent, claims 14, 18, 29; ’602 patent, claim 14; ’984 patent, claim 40; ’140 patent, claims 14, 17, 30, 35.

microprocessor—the 400 Megahertz Pentium II—as an embodiment of a CPU. *See, e.g.*, ’654 patent 6:51-61.

In addition, the extrinsic evidence supports Defendants’ position. For example, the Modern Dictionary of Electronics defines “central processing unit” as:

3. The part of a computer system that controls the interpretation and execution of instructions. In general, the CPU contains the following elements: arithmetic and logic unit (ALU), timing and control, accumulator, scratch-pad memory, program counter and address stack, instruction register, and I/O [input/output] control logic. 4. That unit of a computing system that fetches, decodes, and executes programmed instructions and maintains the status of results as the program is executed.

Ex. 22, at 107. This definition does not include or encompass multiple processing cores. Instead, these components and functions reside in a single CPU core.

Thus, Defendants’ construction is consistent with the specifications of the Asserted Patents as well as the understanding of POSITAs at the relevant time, and should be adopted.

IV. CONCLUSION

Defendants respectfully request that the Court adopt their proposed constructions, which accurately reflect the intrinsic record, and the claims and specifications of the Asserted Patents, whereas ACQIS’s constructions disregard clear definitional statements and disclaimers in both the specification and file histories.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that all counsel of record are being served with a copy of the foregoing document via the Court's CM/ECF system on August 30, 2021.

/s/ J. Stephen Ravel

J. Stephen Ravel